1) Give the mnemonics in order for the 5 cycles if RISC instruction execution.

2) Explain in words what the following instruction does in the second stage of the pipeline. Be sure to include information about what values are stored in the pipeline registers.
   \[ \text{DADD } R4, R2, R3 \]

3) For the 5-stage pipeline, assume that 30\% of all instructions executed cause a single-cycle stall and no other instructions cause any stalls. If forwarding can eliminate 70\% of the stalls, but increases the clock cycle by 10\%, what is the speedup obtained by using forwarding?